

## High Voltage Synchronous Rectified Buck MOSFET Driver

The ISL6209 is a high frequency, dual MOSFET driver, optimized to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter topology in mobile computing applications. This driver, combined with an Intersil Multi-Phase Buck PWM controller, such as ISL6216, ISL6244, and ISL6247, forms a complete single-stage core-voltage regulator solution for advanced mobile microprocessors.

The ISL6209 features 4A typical sink current for the lower gate driver. The 4A typical sink current is capable of holding the lower MOSFET gate during the PHASE node rising edge to prevent the shoot-through power loss caused by the high dv/dt of the PHASE node. The operation voltage matches the 30V breakdown voltage of the MOSFETs commonly used in mobile computer power supplies.

The ISL6209 also features a three-state PWM input that, working together with most of Intersil multiphase PWM controllers, will prevent a negative transient on the output voltage when the output is being shut down. This feature eliminates the Schottky diode, that is usually seen in a microprocessor power system for protecting the microprocessor, from reversed-output-voltage damage.

The ISL6209 has the capacity to efficiently switch power MOSFETs at frequencies up to 2MHz. Each driver is capable of driving a 3000pF load with a 8ns propagation delay and less than a 10ns transition time. This product implements bootstrapping on the upper gate with an internal bootstrap Schottky diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Programmable dead-time with gate threshold monitoring is integrated to prevent both MOSFETs from conducting simultaneously.

### Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”
- Technical Brief TB447 “Guidelines for Preventing Boot-to-Phase Stress on Half-Bridge MOSFET Driver ICs”

## Features

- Drives Two N-Channel MOSFETs
- Shoot-Through Protection
  - Active gate threshold monitoring
  - Programmable dead-time
- 30V Operation Voltage
- 0.4Ω On-Resistance and 4A Sink Current Capability
- Supports High Switching Frequency
  - Fast output rise time
  - Propagation delay 8ns
- Three-State PWM Input for Power Stage Shutdown
- Internal Bootstrap Schottky Diode
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Applications

- Core Voltage Supplies for Intel and AMD® Mobile Microprocessors
- High Frequency Low Profile DC/DC Converters
- High Current Low Output Voltage DC/DC Converters
- High Input Voltage DC/DC Converter

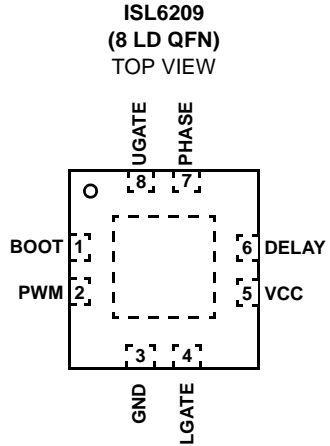
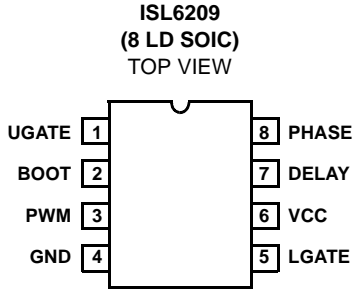
## Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6209CB*	ISL6209CB	-10 to +100	8 Ld SOIC	M8.15
ISL6209CBZ* (Note)	ISL6209CBZ	-10 to +100	8 Ld SOIC (Pb-free)	M8.15
ISL6209CR*	209C	-10 to +100	8 Ld 3x3 QFN	L8.3x3

\*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts



ISL6209 Block Diagram

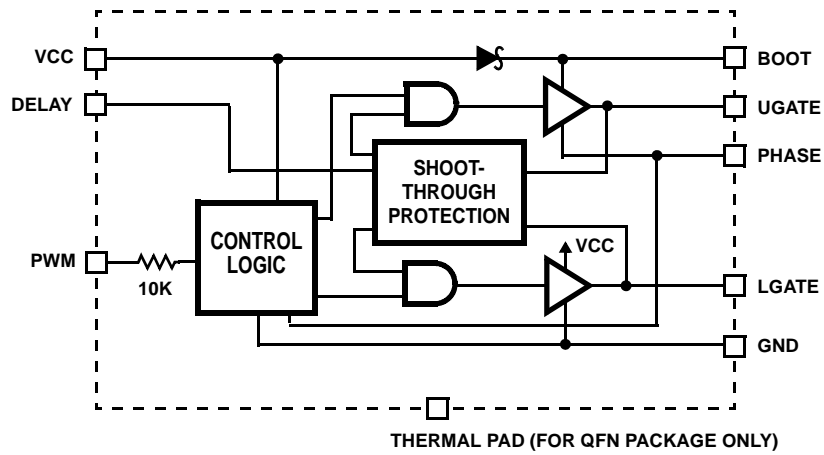
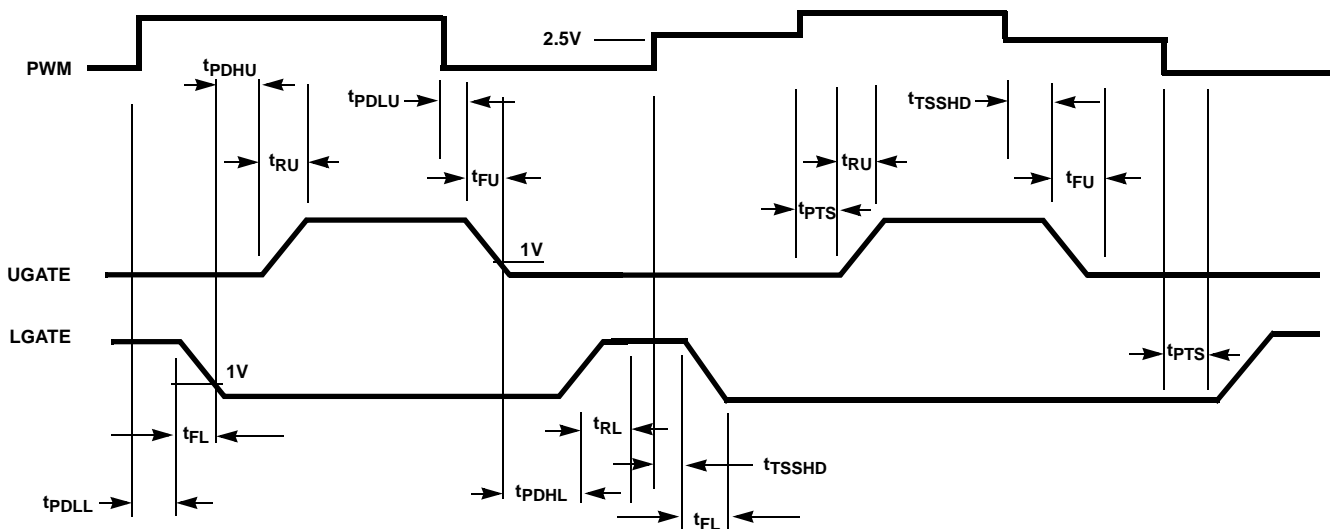


FIGURE 1. BLOCK DIAGRAM

Timing Diagram



Typical Application - Two Phase Converter Using ISL6209 Gate Drivers

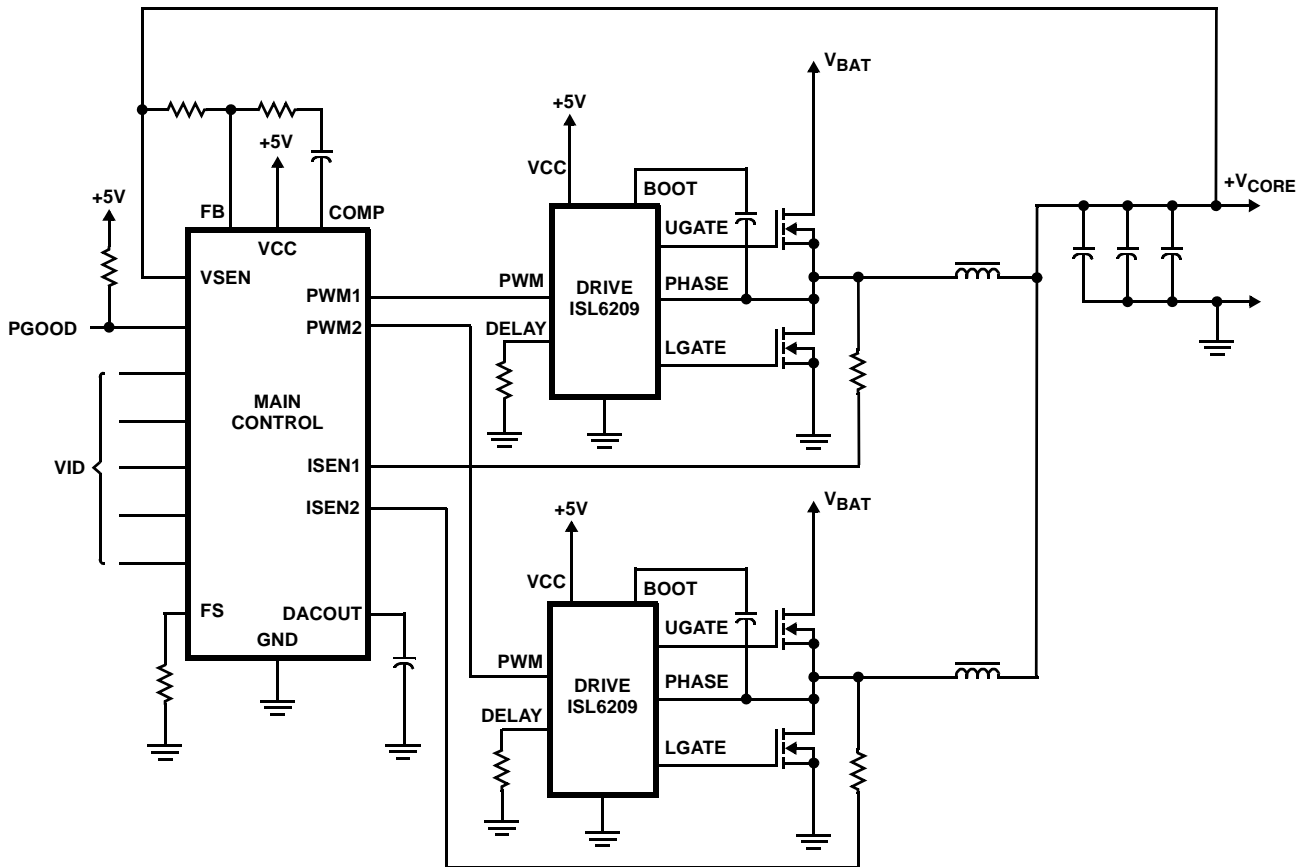


FIGURE 2. TYPICAL APPLICATION

**Absolute Maximum Ratings**

Supply Voltage (VCC)	-0.3V to 7V
Input Voltage (V <sub>DELAY</sub> , V <sub>PWM</sub> )	-0.3V to VCC + 0.3V
BOOT Voltage (V <sub>BOOT-GND</sub> )	-0.3V to 33V
BOOT To PHASE Voltage (V <sub>BOOT-PHASE</sub> )	-0.3V to 7V (DC) -0.3V to 9V (<10ns)
PHASE Voltage (Note 1)	GND - 0.3V to 30V GND - 8V (<20ns Pulse Width, 10μJ)
UGATE Voltage	V <sub>PHASE</sub> - 0.3V (DC) to V <sub>BOOT</sub> V <sub>PHASE</sub> - 5V (<20ns Pulse Width, 10μJ) to V <sub>BOOT</sub>
LGATE Voltage	GND - 0.3V (DC) to VCC + 0.3V GND - 2.5V (<20ns Pulse Width, 5μJ) to VCC + 0.3V
Ambient Temperature Range	-40°C to +125°C

**Recommended Operating Conditions**

Ambient Temperature Range	-10°C to +100°C
Maximum Operating Junction Temperature	+125°C
Supply Voltage, V <sub>CC</sub>	5V ±10%

**Thermal Information**

Thermal Resistance (Typical)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)
SOIC Package (Note 2)	110	N/A
QFN Package (Notes 3, 4)	80	15
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Maximum Lead Temperature (Soldering 10s)	+300°C (SOIC - Lead Tips Only)	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTES:**

- The Phase Voltage is capable of withstanding -7V when the BOOT pin is at GND.
- θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- θ<sub>JA</sub> is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ<sub>JC</sub>, the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>VCC SUPPLY CURRENT</b>						
Bias Supply Current	I <sub>VCC</sub>	PWM pin floating, V <sub>VCC</sub> = 5V	-	85	-	μA
POR Rising			-	3.4	4.2	V
POR Falling			2.2	2.9	-	V
Hysteresis			-	500	-	mV
<b>BOOTSTRAP DIODE</b>						
Forward Voltage	V <sub>F</sub>	V <sub>VCC</sub> = 5V, forward bias current = 2mA	0.40	0.52	0.60	V
<b>PWM INPUT</b>						
Input Current	I <sub>PWM</sub>	V <sub>PWM</sub> = 5V	-	250	-	μA
		V <sub>PWM</sub> = 0V	-	-250	-	μA
PWM Three-State Rising Threshold		V <sub>VCC</sub> = 5V	-	-	1.8	V
PWM Three-State Falling Threshold		V <sub>VCC</sub> = 5V	3.1	-	-	V
Three-State Shutdown Hold-off Time		V <sub>VCC</sub> = 5V, temperature = +25°C	-	150	-	ns
<b>SWITCHING TIME</b>						
UGATE Rise Time (Note 5)	t <sub>RUGATE</sub>	V <sub>VCC</sub> = 5V, 3nF Load	-	8	-	ns
LGATE Rise Time (Note 5)	t <sub>RLGATE</sub>	V <sub>VCC</sub> = 5V, 3nF Load	-	8	-	ns
UGATE Fall Time (Note 5)	t <sub>FUGATE</sub>	V <sub>VCC</sub> = 5V, 3nF Load	-	8	-	ns
LGATE Fall Time (Note 5)	t <sub>FLGATE</sub>	V <sub>VCC</sub> = 5V, 3nF Load	-	4	-	ns
UGATE Turn-Off Propagation Delay	t <sub>PDLUGATE</sub>	V <sub>VCC</sub> = 5V, No Output Load, DELAY = VCC	-	13	-	ns
LGATE Turn-Off Propagation Delay	t <sub>PDLLGATE</sub>	V <sub>VCC</sub> = 5V, No Output Load, DELAY = VCC	-	13	-	ns
UGATE Turn-On Propagation Delay	t <sub>PDHUGATE</sub>	V <sub>VCC</sub> = 5V, Outputs Unloaded, DELAY = VCC	10	20	30	ns

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Noted. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LGATE Turn-On Propagation Delay	$t_{PDHLGATE}$	$V_{VCC} = 5V$ , Outputs Unloaded, DELAY = VCC	10	20	30	ns
<b>OUTPUT</b>						
Upper Drive Source Resistance	$R_{UGATE}$	500mA Source Current	-	1.0	2.5	$\Omega$
Upper Driver Source Current (Note 5)	$I_{UGATE}$	$V_{UGATE-PHASE} = 2.5V$	-	2.0	-	A
Upper Drive Sink Resistance	$R_{UGATE}$	500mA Sink Current	-	1.0	2.5	$\Omega$
Upper Driver Sink Current (Note 5)	$I_{UGATE}$	$V_{UGATE-PHASE} = 2.5V$	-	2.0	-	A
Lower Drive Source Resistance	$R_{LGATE}$	500mA Source Current	-	1.0	2.5	$\Omega$
Lower Driver Source Current (Note 5)	$I_{LGATE}$	$V_{LGATE} = 2.5V$	-	2.0	-	A
Lower Drive Sink Resistance	$R_{LGATE}$	500mA Sink Current	-	0.4	1.0	$\Omega$
Lower Driver Sink Current (Note 5)	$I_{LGATE}$	$V_{LGATE} = 2.5V$	-	4.0	-	A

## NOTE:

5. Guaranteed by characterization, not 100% tested in production.

**Functional Pin Description****UGATE (Pin 1 for SOIC-8, Pin 8 for QFN)**

The UGATE pin is the upper gate drive output. Connect to the gate of high-side power N-Channel MOSFET.

**BOOT (Pin 2 for SOIC-8, Pin 1 for QFN)**

BOOT is the floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Bootstrap Diode and Capacitor section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

**PWM (Pin 3 for SOIC-8, Pin 2 for QFN)**

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller. In addition, place a 500k $\Omega$  resistor to ground from this pin. This allows for proper three-state operation under all start-up conditions.

**GND (Pin 4 for SOIC-8, Pin 3 for QFN)**

GND is the ground pin. All signals are referenced to this node.

**LGATE (Pin 5 for SOIC-8, Pin 4 for QFN)**

LGATE is the lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

**VCC (Pin 6 for SOIC-8, Pin 5 for QFN)**

Connect the VCC pin to a +5V bias supply. Place a high quality bypass capacitor from this pin to GND.

**DELAY (Pin 7 for SOIC-8, Pin 6 for QFN)**

The DELAY pin sets the dead-time between gate switching for the ISL6209. Connect a resistor to GND from this pin to adjust the dead-time, refer to Figure 4. Tie this pin to VCC to disable the delay circuitry. See *Shoot-Through Protection* section for more detail.

**PHASE (Pin 8 for SOIC-8, Pin 7 for QFN)**

Connect the PHASE pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

**Description****Operation**

Designed for speed, the ISL6209 dual MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [ $t_{PDLLGATE}$ ], the lower gate begins to fall. Typical fall times [ $t_{FLGATE}$ ] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [ $t_{PDHUGATE}$ ], based on how quickly the LGATE voltage drops below 1V. This prevents both the lower and upper MOSFETs from conducting simultaneously, or shoot-through. Once this delay period is completed, the upper gate drive begins to rise [ $t_{RUGATE}$ ], and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [ $t_{PDLUGATE}$ ] is encountered before the upper gate begins to fall [ $t_{FUGATE}$ ]. Again, the adaptive

shoot-through circuitry determines the lower gate delay time  $t_{PDHLGATE}$ . The upper MOSFET gate-to-source voltage is monitored, and the lower gate is allowed to rise, after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [ $t_{RLGATE}$ ], turning on the lower MOSFET.

This driver is optimized for converters with large step down ratio, such as those used in a mobile-computer core voltage regulator. The lower MOSFET is usually sized much larger.

This driver is optimized for converters with large step down compared to the upper MOSFET because the lower MOSFET conducts for a much longer time in a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The  $0.4\Omega$  on-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected to the lower gate through the drain-to-gate capacitor of the lower MOSFET and prevent a shoot through caused by the high  $dv/dt$  of the phase node.

**Three-State PWM Input**

A unique feature of the ISL6209 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled. During start-up, PWM should be in the three-state position ( $1/2 V_{CC}$ ) until actively driven by the controller IC.

**Shoot-Through Protection**

The ISL6209 driver delivers shoot-through protection by incorporating gate threshold monitoring and programmable dead-time to prevent upper and lower MOSFETs from conducting simultaneously, thereby shorting the input supply to ground. Gate threshold monitoring ensures that one gate is OFF before the other is allowed to turn ON.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Internal circuitry monitors the upper MOSFET gate-to-source voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

In addition to gate threshold monitoring, a programmable delay between MOSFET switching can be accomplished by placing a resistor from the DELAY pin to ground. This delay allows for maximum design flexibility over MOSFET selection. The delay can be programmed from 5ns to 50ns. If not desired, the DELAY pin must be tied to VCC to disable the delay circuitry. Gate threshold monitoring is not affected

by the addition or removal of the additional dead-time. Refer to Figure 3 and Figure 4 for more detail.

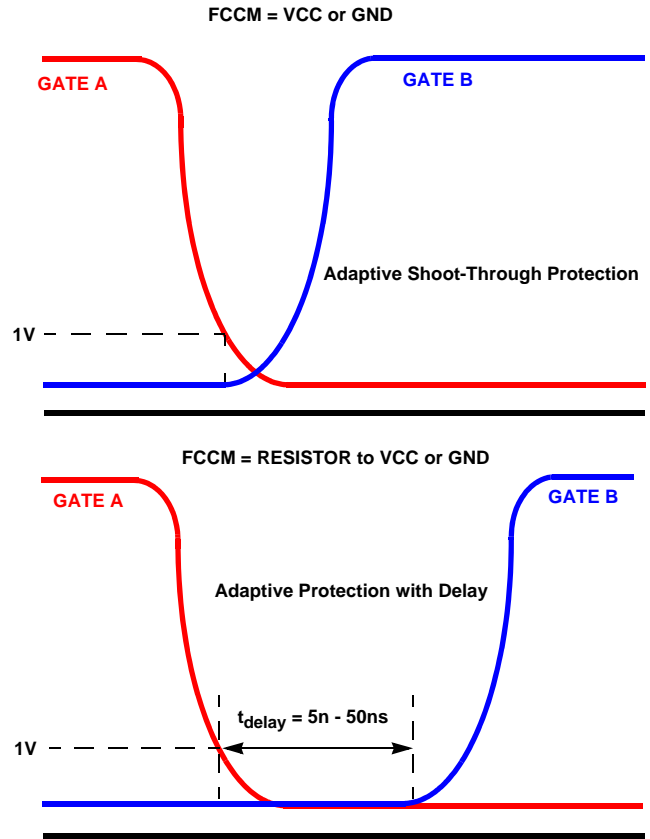


FIGURE 3. PROGRAMMABLE DEAD-TIME

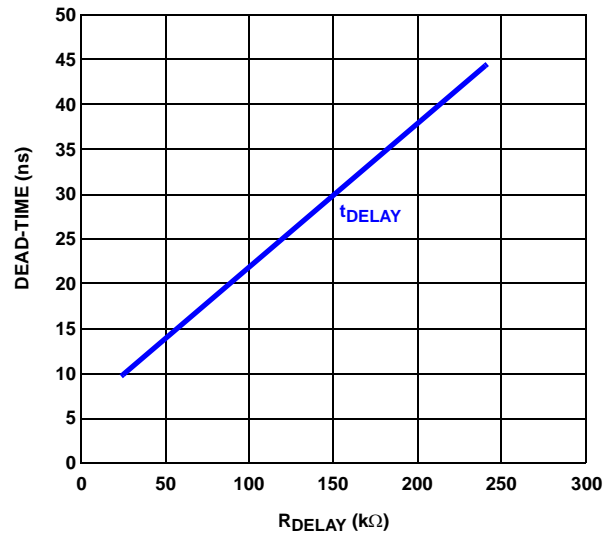


FIGURE 4. ADDITIONAL PROGRAMMED DEAD-TIME ( $t_{DELAY}$ ) vs DELAY RESISTOR VALUE

The equation governing the dead-time seen in Figure 4 is expressed as:

$$T_{\text{DELAY}} = [(160 \times 10^{-15}) \times R_{\text{DELAY}}] + 6\text{ns}$$

The equation can be rewritten to solve for  $R_{\text{DELAY}}$  as follows:

$$R_{\text{DELAY}} = \frac{(T_{\text{DELAY}} - 6\text{ns})}{160 \times 10^{-15}}$$

### Internal Bootstrap Diode

This driver features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above the maximum battery voltage plus 5V. The bootstrap capacitor can be chosen from the following equation:

$$C_{\text{BOOT}} \geq \frac{Q_{\text{GATE}}}{\Delta V_{\text{BOOT}}}$$

where  $Q_{\text{GATE}}$  is the amount of gate charge required to fully charge the gate of the upper MOSFET. The  $\Delta V_{\text{BOOT}}$  term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge,  $Q_{\text{GATE}}$ , of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125 $\mu$ F is required. The next larger standard value capacitance is 0.22 $\mu$ F. A good quality ceramic capacitor is recommended.

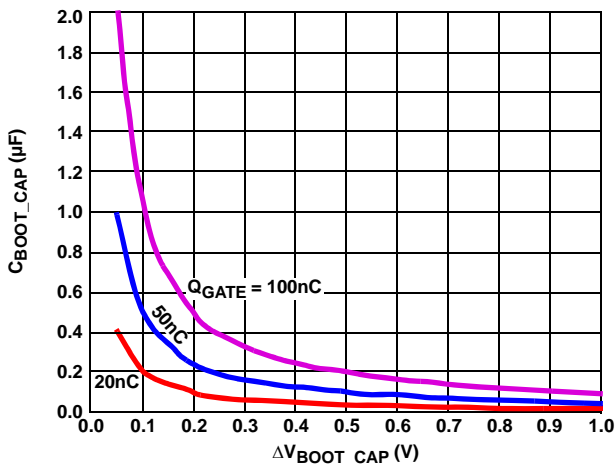


FIGURE 5. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

### Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level

will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO-8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as:

$$P = f_{\text{sw}}(1.5V_{\text{U}}Q_{\text{U}} + V_{\text{L}}Q_{\text{L}}) + I_{\text{VCC}}V_{\text{CC}}$$

where  $f_{\text{sw}}$  is the switching frequency of the PWM signal.  $V_{\text{U}}$  and  $V_{\text{L}}$  represent the upper and lower gate rail voltage.  $Q_{\text{U}}$  and  $Q_{\text{L}}$  is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The  $I_{\text{VCC}}V_{\text{CC}}$  product is the quiescent power of the driver and is typically negligible.

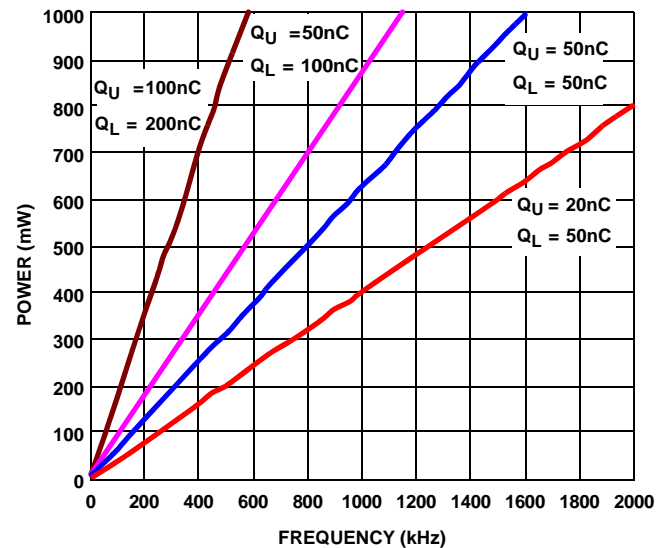


FIGURE 6. POWER DISSIPATION vs FREQUENCY

### Layout Considerations

#### Reducing Phase Ring

The parasitic inductances of the PCB and power devices (both upper and lower FETs) could cause increased PHASE ringing, which may lead to voltages that exceed the absolute maximum rating of the devices. When PHASE rings below ground, the negative voltage could add charge to the bootstrap capacitor through the internal bootstrap diode. Under worst-case conditions, the added charge could overstress the BOOT and/or PHASE pins. To prevent this from happening, the user should perform a careful layout inspection to reduce trace inductances, and select low lead inductance MOSFETs and drivers. D<sup>2</sup>PAK and DPAK packaged MOSFETs have high parasitic lead inductances, as opposed to SOIC-8. If higher inductance MOSFETs must be used, a Schottky diode is recommended across the lower MOSFET to clamp negative PHASE ring.

A good layout would help reduce the ringing on the phase and gatenodes significantly:

1. Avoid using vias for decoupling components where possible, especially in the BOOT-to-PHASE path. Little or no use of vias for VCC and GND is also recommended. Decoupling loops should be short.
2. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, and avoid using vias. If vias must be used, two or more vias per layer transition is recommended.
3. Keep the SOURCE of the upper FET as close as thermally possible to the DRAIN of the lower FET.
4. Keep the connection in between the SOURCE of lower FET and power ground wide and short.
5. Input capacitors should be placed as close to the DRAIN of the upper FET and the SOURCE of the lower FET as thermally possible.

NOTE: Refer to Intersil Tech Brief TB447 for more information.

### ***Thermal Management***

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal pad of the QFN part to the power ground with multiple vias, or placing a low noise copper plane underneath the SOIC part is recommended. This heat spreading allows the part to achieve its full thermal potential.

### ***Suppressing MOSFET Gate Leakage***

With VCC at ground potential, UGATE and LGATE are high impedance. In this state, any stray leakage has the potential to deliver charge to either gate. If UGATE receives sufficient charge to bias the device on (Note: Internal circuitry prevents leakage currents from charging above 1.8V), a low impedance path will be connected between the MOSFET drain and PHASE. If the input power supply is present and active, the system could see potentially damaging currents. Worst-case leakage currents are on the order of pico-amps; therefore, a 10k $\Omega$  resistor, connected from UGATE to PHASE, is more than sufficient to bleed off any stray leakage current. This resistor will not affect the normal performance of the driver or reduce its efficiency.

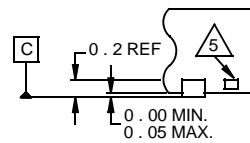
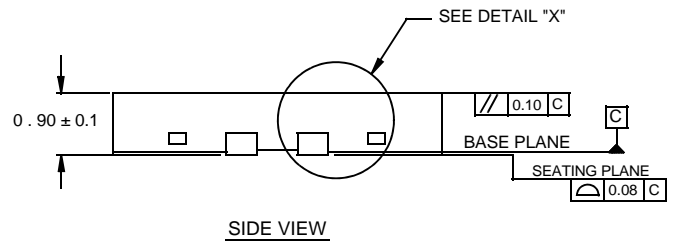
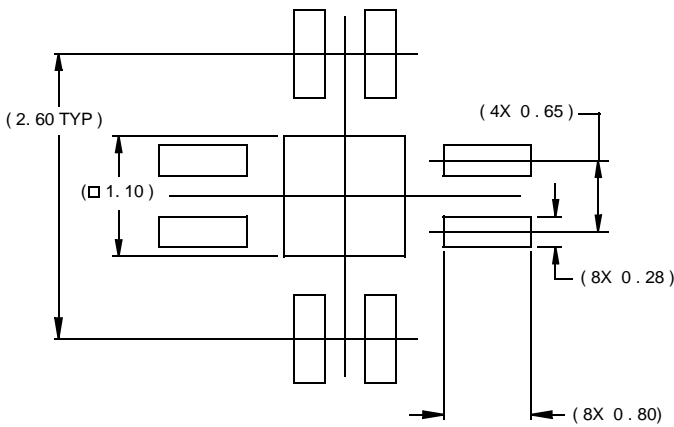
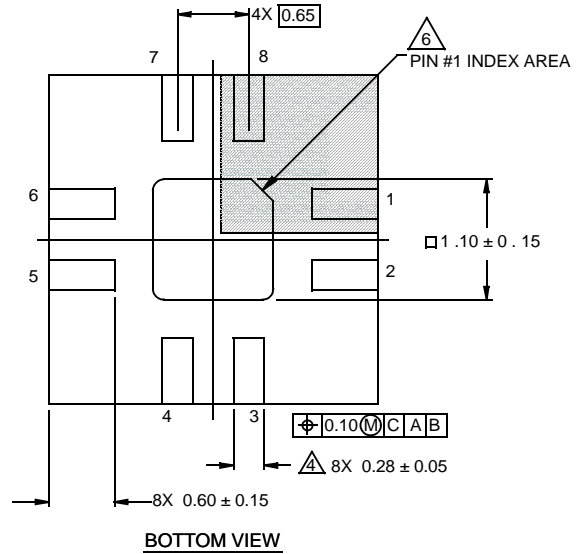
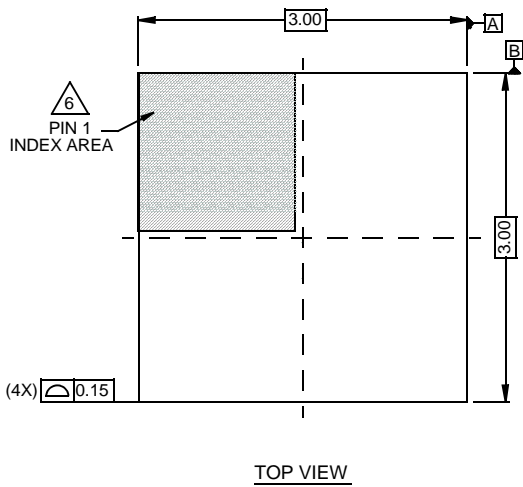


# Package Outline Drawing

## L8.3x3

8 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

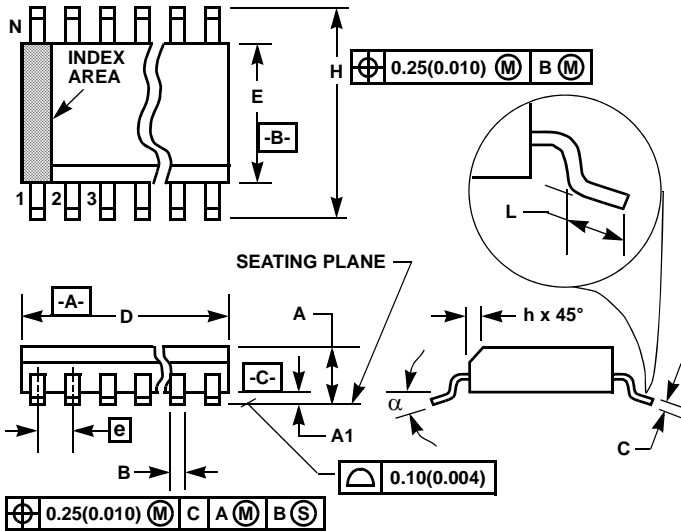
Rev 2, 3/07



NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)  
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
$\alpha$	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 6/05

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